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EXAMINER

NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
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2614

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

11/24/04

Office Action Summary

Application No.

09/905,392

Applicant(s)

MORRISH, ANDY

Examiner

Paulos M. Natnael

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19-21 is/are allowed.
- 6) ☒ Claim(s) 1-7 and 9-18 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of: _____
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims **1-7, 9-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, U.S. Patent No. 6,486,919.

Considering claim 1, Kim discloses the following claimed subject matter, note;

a) the claimed a clock signal generator that is configured to produce multiple horizontal clock signals in response to the horizontal flyback signal, wherein each multiple horizontal clock signal has a different phase with respect to one another, is **implied** here because the Horizontal synchronous signals, HS12, HD, and HS1 which are inputted to the phase difference circuits 2 and 18, and horizontal driving signal generator 6 as shown in Fig.3 have to be generated somewhere.

b) a phase selection circuit that is configured to select one of the multiple horizontal clock signals such that an edge associated with the selected multiple horizontal clock

signal is non-coincident with an edge associated with the vertical flyback signal, is met by First and Second Phase Difference Detectors 18 and 2, respectively, fig.3;

Except for;

c) a blanking circuit that is configured [to] produce a blanking signal in response to the selected multiple horizontal clock signal such that the blanking signal determines the vertical position of the OSD image, whereby noise effects associated with at least one of the vertical flyback signal and the horizontal flyback signal are minimized.

Regarding c), Kim discloses that the horizontal driving signal generator 6 generates an HD signal in response to the flyback signal (FBP) from circuit 2. Kim does not specifically disclose generating a blanking signal. However, Examiner takes Official Notice here in that generation of the vertical blanking signal for position control is well known in the art and, therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Kim by providing the notoriously well-known blanking signal pulses in order to control the position of the image on the screen.

Considering claim 2, the apparatus of Claim 1, wherein the horizontal clock signal generator produces the multiple horizontal clock signals in response to a horizontal rate signal and a scaled horizontal rate signal that is produced by a phase-locked loop circuit, wherein the scaled horizontal rate signal has a frequency that is a multiple of another frequency that corresponds to the horizontal rate signal;

See rejection of claim 1(a);

Considering claim 3, the apparatus of Claim 2, wherein the phase-locked loop circuit produces at least one of the horizontal rate signal and the scaled horizontal rate signal in response to the horizontal flyback signal, is implied because the clock inputs to the various devices in fig.3 are produced by a PLL circuit.

Considering claim 4, the apparatus of Claim 2, wherein the scaled horizontal rate signal has a scaled frequency that is double another frequency that corresponds to the horizontal rate signal, is implied because the frequency has been scale and therefore the result would contribute to the doubling of the frequency.

Considering claim 5, the apparatus of Claim 2, wherein the horizontal rate signal and the scaled horizontal rate signal are dependent upon a predetermined resolution of the display device.

See rejection of claim 2;

Considering claim 6, the apparatus of Claim 1, further comprising an interlace correction circuit that is arranged to selectively shift the phase of the multiple horizontal clock signals between each vertical frame period to compensate for a one-half line shift in the edge of the vertical flyback signal that occurs when the display device is in an interlace mode.

Regarding claim 6, Kim does not specifically disclose an interlace correction circuit. However, Examiner takes Official Notice here in that interlace correction or conversion is well known in the art, and therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Kim by providing the notoriously well-known interlace correction circuit in order to appropriately display signals on the display device.

Considering claim 7, the apparatus of Claim 6, wherein the interlace correction circuit produces an interlace phase shift signal that is utilized by the clock signal generator to change the phase of each of the multiple horizontal clock signals.

See rejection of claim 6.

Considering claim 9, the apparatus of Claim 1, the phase selection circuit further comprising a combinational logic circuit that is configured to produce logic outputs that determine the selection of one of the multiple horizontal clock signals, is met by the phase difference detector 18 (fig.3) which includes an DLL, a bit converter and latch circuit.

Considering claim 10, the apparatus of Claim 9, wherein the combinational logic circuit produces the logic outputs dependent upon a previous selection of one of the multiple horizontal clock signals.

See rejection of claim 9.

Considering claim **11**, the apparatus of Claim 1, wherein each adjacent multiple horizontal clock signal is substantially separated by 90 degrees, is met by HSI2, HD, and HIS, fig.3;

Considering claim **12**, the apparatus of Claim 1, wherein the vertical position of the OSD image is positioned within a display screen of the display device corresponding to a predetermined number of horizontal lines from a starting position on the display screen in response to the blanking signal.

See rejection of claim 1 (c).

Claim **13** is a method claim of Claim 1, and thus, Claim **13** is rejected for the same reason as in claim 1.

Considering claim **14**, the method of Claim 13, further comprising generating one of the first horizontal timing signal and the second horizontal timing signal by a phase-locked loop circuit in response to a horizontal flyback signal of the display device.

See rejection of claim 3;

Considering claim **15**, the method of Claim 13, further comprising correcting the phase of each of the multiple horizontal clock signals for when the display device is operating in an interlace mode.

See rejection of claim 6;

Considering claim 16, the method of Claim 15, further comprising shifting the phase of each of the multiple horizontal clock signals by 180 degrees between each vertical frame period to compensate for a one-half line delay in the edge of the vertical flyback signal that occurs between each vertical frame period when the display device is operating in the interlace mode.

See rejection of claim 11;

Considering claim 17, the method of Claim 13, wherein selecting one of the multiple horizontal clock signals further comprises selecting one of the multiple horizontal clock signals depending on the multiple horizontal clock signal selected for a previous occurrence of the vertical flyback signal, is met by the phase difference detector 18, fig.3;

Considering claim 18, the method of Claim 13, wherein producing multiple horizontal clock signals further comprises producing each multiple horizontal clock signal such that each multiple horizontal clock signal has a phase that is 90 degrees apart from each adjacent multiple horizontal clock signal.

See rejection claim 11.

Response to Arguments

3. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claims 19-21 are allowable over the prior art.

5. Claims 8, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose, an apparatus for reducing noise effects associated with the vertical position of an OSD image for a display device that uses a vertical flyback signal and horizontal flyback signal in producing an image, comprising: wherein the selected horizontal clock signal has an associated clock period, and the selected horizontal clock signal is selected such that the edge associated with the selected horizontal clock signal occurs at least one quarter of the clock period apart from the vertical flyback signal, as in claim 8;

An apparatus for providing jitter reduction for an on screen display (OSD) window of a display device having a display screen, comprising: a means for generating horizontal timing signal that is configured to generate a first horizontal timing signal and a second horizontal timing signal, the first horizontal timing signal and the second horizontal timing signal are related; a means for producing multiple horizontal clock

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signals that is configured to produce multiple horizontal clock signals in response to the horizontal timing signal and the second horizontal timing signal such that each of the multiple horizontal clock signals has a different phase; a means for selecting a multiple horizontal clock signal that is configured to select one of the multiple horizontal clock signals such that the occurrence of an edge corresponding to the selected horizontal clock signal is non-coincident with an edge associated with the vertical flyback signal; and a means for producing a vertical blanking signal that is configured to produce a vertical blanking signal in response to the selected horizontal clock signal wherein the vertical blanking signal triggers the display device to count a predetermined number of blank horizontal lines from the top of the display screen prior to generating the OSD image such that the predetermined number of blank horizontal lines corresponds to the vertical position of the OSD image on the display screen, whereby jitter in the vertical position of the OSD window is reduced, as in claim 19;

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



PAULOS M. NATNAEL
PATENT EXAMINER

PMN
January 10, 2005